

## IN THE CLAIMS

Please make the following amendments to the claims:

1. (Currently Amended) A power-up circuit of a semiconductor memory device, comprising:

a power supply voltage level follower unit for providing a bias voltage which is linearly varied according to variation of a power supply voltage;

a power supply voltage detection unit for detecting ~~the variation whether a~~ voltage level of the power supply voltage ~~to reaches~~ a predetermined critical voltage level in response to the bias voltage to thereby generate a detection signal; and

a reset prevention unit ~~for canceling variation of the detection signal due to a power drop by delaying level transition of the detection signal according to decrease of the power supply voltage generating a power-up signal by performing a pull-down operation controlled by the detection signal and a delayed detection signal to thereby prevent a logic level of the power-up signal from transitioning during a power drop of the power supply voltage, wherein the delayed detection signal is generated by~~ delaying the detection signal.

2. (Currently Amended) The power-up circuit as recited in claim 1, further comprising a buffer unit for outputting ~~at the~~ a power-up signal by buffering an output signal of the reset prevention unit the detection signal.

3. (Currently Amended) The power-up circuit as recited in claim 1, wherein the reset prevention unit includes:

a first pull-up means and a first pull-down means controlled by ~~an output signal of the power supply voltage detection unit~~ the detection signal; and

a response delaying means for delaying ~~an a~~ a pull-up operation of the first pull-up means according to a transition of the output signal of the power supply voltage detection unit detection signal.

4. (Currently Amended) The power-up circuit as recited in claim 3, wherein the response delay means includes:
- a delay unit for delaying the ~~output signal of the power supply voltage detection unit~~ detection signal by a predetermined time; and
  - a second pull-up means connected between the first pull-up means and a power supply voltage, and controlled by an output signal of the delay unit.
5. (Original) The power-up circuit as recited in claim 4, wherein the predetermined time for delaying the output signal of the power supply voltage detection unit in the delay unit is longer than a time that the detection signal is maintained in a logic low level due to the power drop.
6. (Original) The power-up circuit as recited in claim 4, wherein the reset prevention unit further includes an inverter connected to the first pull-up means and the first pull-down means.
7. (Currently Amended) The power-up circuit as recited in claim 4, wherein each of the first and second pull-up means ~~are~~ is a PMOS transistor, and the pull-down means is an NMOS transistor.
8. (Currently Amended) The power-up circuit as recited in claim 4, wherein the power supply voltage level follower unit is provided between the power supply voltage and a ground voltage, and includes a first and a second load elements ~~configuring~~ configured as a voltage divider.
9. (Currently Amended) The power-up circuit as recited in claim 4, wherein the power supply voltage detection unit includes:
- a load element connected between the power supply voltage and a first node;
  - an NMOS transistor which is connected between a ground voltage and the first node and whose gate receives a the bias voltage; and

an inverter, which is connected to the first node, for outputting the detection signal.

10. (Original) The power-up circuit as recited in claim 9, wherein the load element is a PMOS transistor which is connected between the power supply voltage and the first node, and whose gate is connected to the ground voltage.

11. (Original) The power-up circuit as recited in claim 2, wherein the buffer unit includes an inverter chain receiving an output signal of the reset prevention unit.

12. (New) A power initialization circuit for a semiconductor memory device, comprising:

a power supply voltage level follower unit to provide a bias voltage which varies linearly with a power supply voltage;

a power supply voltage detection unit to detect when a level of the power supply voltage reaches a predetermined level; and

a reset prevention unit to generate a power-up signal, the reset prevention unit including two pull-up devices in series with a pull-down device, the pull-down device and one pull-up device controlled by a signal from the power supply voltage detection unit and one pull-up device controlled by a delayed version of the signal from the power supply voltage detection unit.